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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,637	11/06/2001	Govind Kizhepat	GKIZ 1000-1	5830

22470 7590 01/08/2007
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EXAMINER	
STEVENS, ROBERT	
ART UNIT	PAPER NUMBER
2162	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/992,637	KIZHEPAT, GOVIND	
	Examiner	Art Unit	
	Robert Stevens	2162	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Office maintains/withdraws the previous rejections of the claims under 35 USC §§ 112-1st paragraph and 103(a), in light of the amendment. However, the Office sets forth new rejections of the claims under 35 USC §103(a), in light of the amendment.

Response to Arguments

2. Applicant's arguments with respect to claims 1-33 have been considered but are moot in view of the new ground(s) of rejection.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/16/2006 has been entered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-33 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Bartkowiak et al. (US Patent No. 5,771,362, filed May 17, 1996 and issued Jun. 23, 1998, hereafter referred to as "Bartkowiak") in view of Wang et al. (US Patent No. 7,028,134, filed Dec. 28, 2000 and issued Apr. 11, 2006, hereafter referred to as "Wang").

Regarding independent claim 1: Bartkowiak teaches ***A data processing system, comprising: a plurality of functional units having respective inputs and outputs, and adapted to perform respective tasks using input data at the respective inputs and to supply output data at the respective outputs, within a cycle;*** (See Bartkowiak Abstract, discussing the routing of data among functional units.) ***and control word distribution circuitry which supplies the routing control signals in parallel to the plurality of routing units to establish a route for a cycle, where the route includes applying data output in the cycle by a first functional unit in the plurality of functional units as input in the function cycle to a second functional unit in the plurality of functional units, and applying data output by the second functional unit in the cycle as input in the cycle to a third functional unit in the cycle.*** (See Bartkowiak col. 2 lines 15-32, discussing a dynamically configurable interconnect, in which an instruction filed specifies the interconnect configuration.)

However, Bartkowiak does not explicitly teach the further limitations as claimed. Wang, though, discloses ***a plurality of routing units, responsive to respective routing control signals, by which data is steered among inputs and outputs of the plurality of functional units, routing units in the plurality of routing units being coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets is different***

than another of said respective subsets; (See Wang Abstract and Figure 3, teaching a plurality of crossbar switches in which the switches receive communications and a clock signal via parallel channels.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Wang for the benefit of Bartkowiak, because to do so allowed a system designer to reduce power consumption and footprint required to provide synchronized clocking, as taught by Wang in col. 3 lines 1-6. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Regarding claim 2: Bartkowiak does not explicitly teach the remaining limitations as claimed. Wang, though, discloses ***wherein said plurality of routing units includes at least one multiplexer having a plurality of inputs and coupled to respective functional units in the plurality of functional units and at least one output coupled to a functional unit in the plurality of functional units, and the routing control signal for the multiplexer specifies one of a plurality of inputs to indicate a source functional unit, and one of the at least one outputs to indicate a destination functional unit.*** (See Wang Figure 7 showing 8 multiplexer chips, in the context of col. 2 lines 15-32 which discusses a dynamically configurable interconnect, in which an instruction filed specifies the interconnect configuration.)

Regarding claim 3: Bartkowiak does not explicitly teach the remaining limitations as claimed. Wang, though, discloses ***wherein said plurality of routing units includes at least one crossbar switch.*** (See Wang Figure 7, showing 2 crossbar chips.)

Regarding claim 4: Bartkowiak teaches ***wherein said plurality of functional units includes at least one storage element***. (See Bartkowiak Abstract and col. 4 lines 40-50, teaching the routing of data to/from memory.)

Regarding claim 5: Bartkowiak teaches ***wherein said plurality of functional units includes at least one logic block which performs a plurality of available functions, and includes logic to select an output from one of the plurality of available functions in response to a routing control signal***. (See Bartkowiak col. 3 lines 52-65, discussing functional unit configurations in a DSP and describing functional units as a block of circuitry to perform at least one operation.)

Regarding claim 6: Bartkowiak teaches ***wherein said plurality of functional units includes a memory responsive to addresses, write control signals, and read control signals, and the control word distribution circuitry supplies at least one of the write control signals and read control signals***. (See Bartkowiak col. 4 lines 40-50 teaching the use of addresses in performing read/write operations, in the context of the Abstract which discusses routing among functional units.)

Regarding claim 7: Bartkowiak teaches ***wherein the control word distribution circuitry supplies an address for said memory***. (See Bartkowiak col. 4 lines 40-50, teaching the use of addresses in performing read/write operations.)

Regarding claim 8: Bartkowiak teaches ***wherein an address for said memory is supplied by one of the plurality of functional units***. (See Bartkowiak col. 5 lines 34-50, discussing a MAC functional unit coupled to input and output registers.)

Regarding claim 9: Bartkowiak teaches ***wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks***. (See Bartkowiak col. 3 lines 52-65, discussing a functional unit block of circuitry to perform operations.)

Regarding claim 10: Bartkowiak teaches ***wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks***. (See Bartkowiak col. 3 lines 52-65, discussing a functional unit block of circuitry to perform operations.)

Regarding claim 11: Bartkowiak teaches ***wherein said control word distribution circuitry supplies said routing control signals synchronously to the plurality of routing units***. (See Bartkowiak col. 4 lines 42-44, discussing the use of control signals during a clock cycle to set up a route to a storage location.)

Regarding independent claim 12: Bartkowiak teaches ***A data processing system, comprising: a plurality of processing blocks having respective inputs and outputs, and adapted to perform respective processes using input data at the respective inputs and to supply output data at the respective outputs, within a function cycle;*** (See Bartkowiak Abstract, discussing the routing of data among functional units.) ***and block level control word distribution circuitry which supplies control words for respective cycles to the plurality of routing units, said control words including the routing control signals for the plurality of routing units;*** (See Bartkowiak Abstract, discussing the use of an instruction field to set up interconnect configurations during a clock cycle.) ***wherein processing blocks in said plurality of processing blocks respectively include a plurality of functional units having respective inputs and outputs, and adapted to perform respective processes using input data at the respective inputs and to supply output data at the respective outputs, within a block cycle;*** (See Bartkowiak Abstract, discussing the routing of data from a functional unit to memory, it having been implicit that such data was first input into the functional unit.) ***and functional unit level control word distribution circuitry which supplies control words for respective block cycles to the plurality of unit level routing units, said control words including the routing control signals to establish a route in the block cycle for the plurality of unit level routing units, where the route includes applying data output in the block cycle by a first functional unit in the plurality of functional units as input in the block cycle to a second functional unit in the plurality of functional units, and applying data output by the second functional unit in the block cycle as input in the block cycle to a third functional unit in the block function cycle.*** (See Bartkowiak col. 2 lines 15-32,

discussing a dynamically configurable interconnect, in which an instruction filed specifies the interconnect configuration.)

However, Bartkowiak does not explicitly teach the further limitations as claimed. Wang, though, discloses ***a plurality of routing units, responsive to respective routing control signals for the plurality of processing blocks, by which data is steered among the inputs and outputs of the plurality of processing blocks, routing units in the plurality of routing units being coupled to respective subsets of processing blocks in the plurality of processing blocks, wherein at least one of said respective subsets of processing blocks is different than another of said respective subsets processing blocks;*** (See Wang Abstract and Figure 3, teaching a plurality of crossbar switches in which the switches receive communications and a clock signal via parallel channels.) ***a plurality of unit level routing units, coupled to the plurality of functional units and responsive to respective routing control signals for the plurality of unit level routing units, by which data is steered among the inputs and outputs of the plurality of functional units, unit level routing units in the plurality of unit level routing units being coupled to respective subsets of functional units in the plurality of functional unit, wherein at least one of said respective subsets of functional units is different than another of said respective subsets of functional units;*** (See Wang Figure 7 and col. 5 line 59 – col. 6 line2, teaching the interconnections and routing among functional units, such as queues, and routing units, such as multiplexers and crossbars.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Wang for the benefit of Bartkowiak, because to do so allowed a system designer to reduce power consumption and footprint required to provide synchronized clocking,

as taught by Wang in col. 3 lines 1-6. These references were all applicable to the same field of endeavor, i.e., workflow management.

Claims 13-22 are substantially similar to claims 2-11, respectively, and therefore likewise rejected.

Regarding independent claim 23: Bartkowiak teaches ***A method of processing data, in a data processing engine that includes a plurality of functional units,*** (See Bartkowiak Abstract, discussing data processing including functional units.) ***comprising: providing a set of software routing control signals in parallel to a set of routing units in the data processing engine to specify a route for a cycle among the plurality of functional units;*** (See Bartkowiak Abstract, discussing the specifying of interconnect configurations during a clock cycle.)

However, Bartkowiak does not explicitly teach the further limitations as claimed. Wang, though, discloses ***and routing data among the plurality of functional units according to the set of software routing control signals and performing tasks in the plurality of functional units using the route to produce a result, wherein routing units in the set of routing units are coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets of functional units is different than another of said respective subsets of functional units, where the route includes applying data output in the cycle by a first functional unit in the plurality of functional units as input in the cycle to a second functional unit in the plurality of functional units, and applying data output by the second functional unit in the cycle as input in the function cycle to a third functional unit in***

the cycle. (See Wang Abstract and Figure 3 teaching a plurality of crossbar switches in which the switches receive communications and a clock signal via parallel channels, and Figure 7 and col. 5 line 59 – col. 6 line2 teaching the interconnections and routing among functional units, such as queues, and routing units, such as multiplexers and crossbars.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Wang for the benefit of Bartkowiak, because to do so allowed a system designer to reduce power consumption and footprint required to provide synchronized clocking, as taught by Wang in col. 3 lines 1-6. These references were all applicable to the same field of endeavor, i.e., workflow management.

Regarding claim 24: Bartkowiak teaches ***compiling a high level programming language specifying the result to produce the set of software routing control signals.*** (See Bartkowiak Abstract, discussing the use of programmer code to implement routing algorithms.)

Claims 25-26 are substantially similar to claims 9-10, respectively, and therefore likewise rejected.

Regarding claim 27: Bartkowiak teaches ***wherein the routing units in the data processing engine comprise a plurality of switches interconnecting the plurality of functional units, and said set of routing control signals specify data paths through the plurality of switches.*** (See Bartkowiak Abstract, discussing dynamically establishing data path configurations.)

Regarding claim 28: Bartkowiak teaches ***including synchronously routing said data among the plurality of functional units***. (See Bartkowiak Abstract, discussing routing during a clock cycle.)

Regarding independent claim 29: Bartkowiak teaches ***A method of processing data in a data processing engine that includes a plurality of functional units,*** (See Bartkowiak Abstract, discussing data processing including functional units.) ***comprising: performing tasks in said plurality of functional units using the first data path in the first cycle;*** (See Bartkowiak Abstract and col. 3 lines 53-65, teaching establishing interconnect paths among functional units to perform operations.) ***and performing tasks in said plurality of functional units using the second data path to accomplish said different function in the second cycle.*** (See Bartkowiak Abstract and col. 3 lines 53-65, teaching establishing interconnect paths among functional units to perform operations.)

However, Bartkowiak does not explicitly teach the further limitations as claimed. Wang, though, discloses ***providing a first set of software routing control signals in parallel to a set of routing units in the data processing engine to specify a first data path according to a first configuration of the first cycle, wherein routing units in the set of routing units are coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets of functional units is different than another of said respective subsets of functional units, where the first data path includes applying data output in the first cycle by a first functional unit in the plurality of functional units as input in the first cycle to a***

second functional unit in the plurality of functional units, and applying data output by the second functional unit in the first cycle as input in the first cycle to a third functional unit in the first cycle; (See Wang Abstract and Figure 3 teaching a plurality of crossbar switches in which the switches receive communications and a clock signal via parallel channels, and Figure 7 and col. 5 line 59 – col. 6 line2 teaching the interconnections and routing among functional units, such as queues, and routing units, such as multiplexers and crossbars.) ***providing a second set of software routing control signals in parallel to said set of routing units to specify a second data path according to a second configuration of the plurality of functional units for a second cycle, whereby the plurality of functional units is reconfigured to perform a different function;*** (See Wang Abstract and Figure 3 teaching a plurality of crossbar switches in which the switches receive communications and a clock signal via parallel channels, and Figure 7 and col. 5 line 59 – col. 6 line2 teaching the interconnections and routing among functional units, such as queues, and routing units, such as multiplexers and crossbars.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Wang for the benefit of Bartkowiak, because to do so allowed a system designer to reduce power consumption and footprint required to provide synchronized clocking, as taught by Wang in col. 3 lines 1-6. These references were all applicable to the same field of endeavor, i.e., workflow management.

Claims 30-31, 32 and 33 are substantially similar to claims 9-10, 27 and 24, respectively, and therefore likewise rejected.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent Application Publications

Marmash	2003/0191879

US Patents

McWilliams et al	7,043,596
Han et al	6,055,599
MacLellan et al	6,636,933
Okazawa et al	6,378,021
Sheafor et al	6,223,242
Hahn et al	6,314,487
Purcell et al	6,836,815
Osaka et al	6,842,104
Venkitakrishnan	6,263,415
Venkitakrishnan	6,597,692
Bauman	6,799,252
Van Loo et al	5,907,485
Chalasani et al	5,274,782
Wong et al	5,530,814
Taylor	5,313,590

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert Stevens whose telephone number is (571) 272-4102. The examiner can normally be reached on M-F 6:00 - 2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Breene can be reached on (571) 272-4107. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert Stevens
Examiner
Art Unit 2162

January 3, 2007

MOHAMMAD ALI
PRIMARY EXAMINER